

FIG. 1

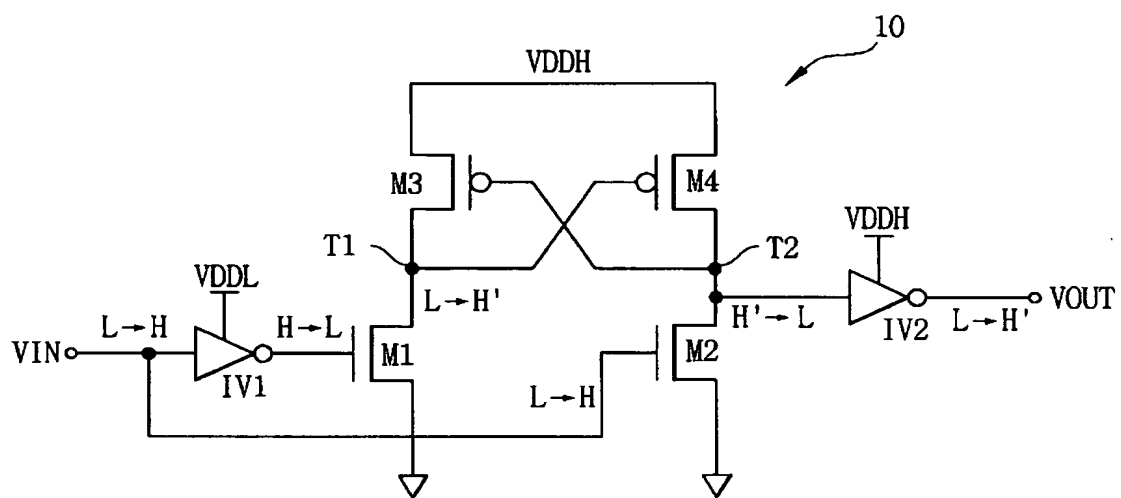


FIG. 2

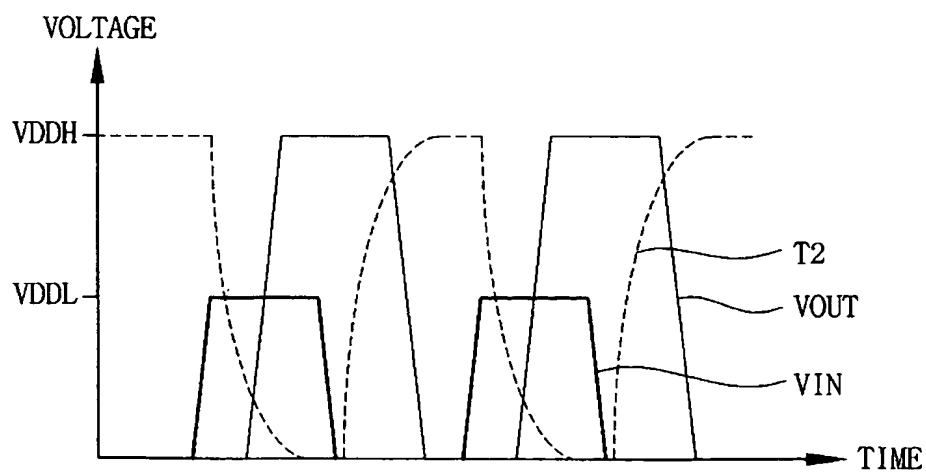


FIG. 3  
(PRIOR ART)

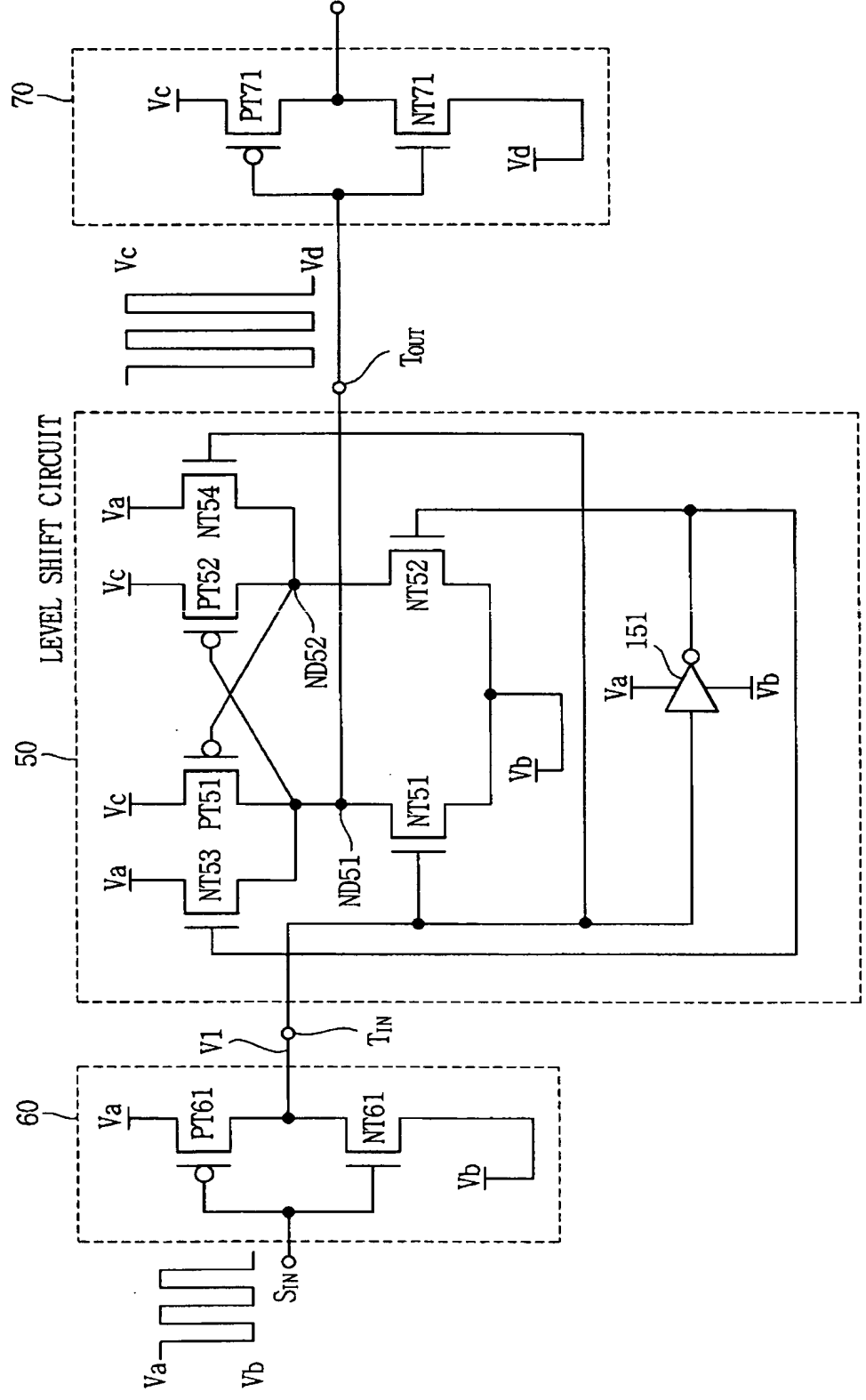


FIG. 4

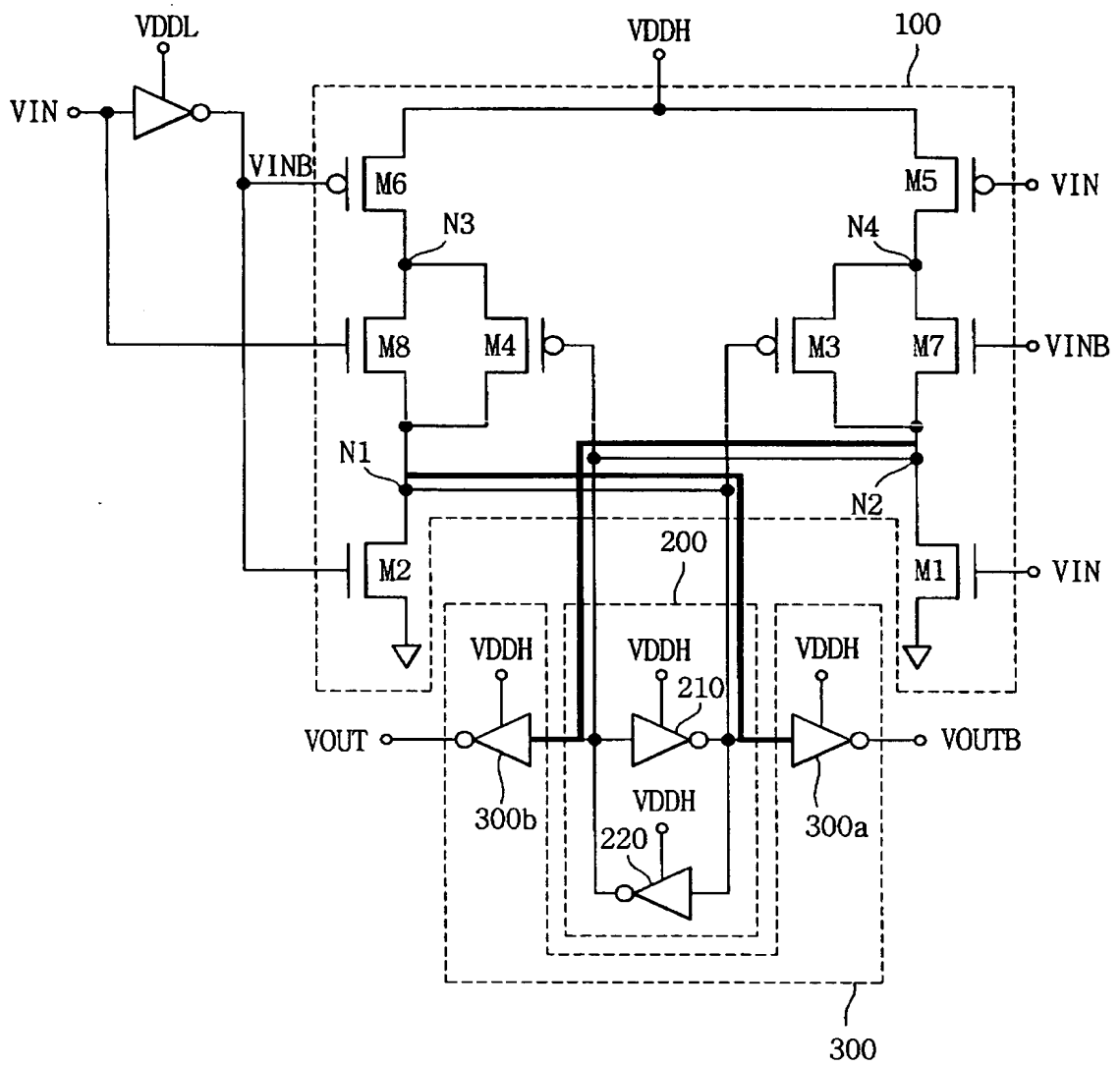


FIG. 5A

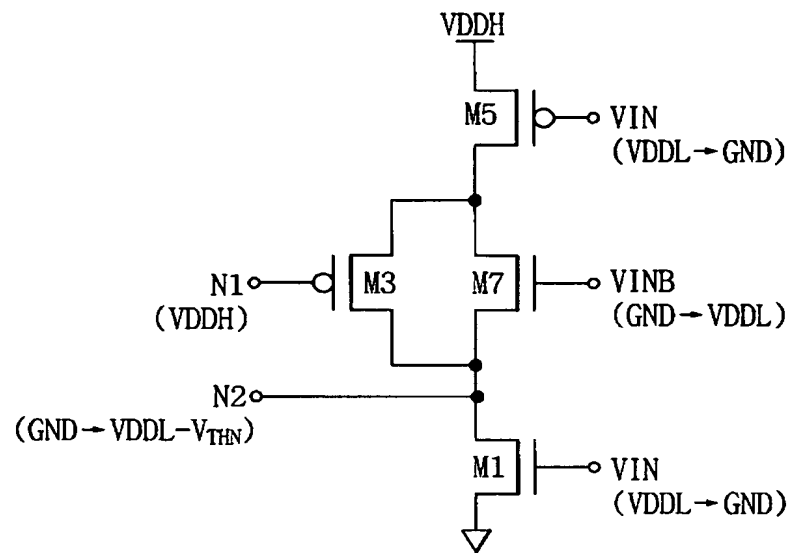


FIG. 5B

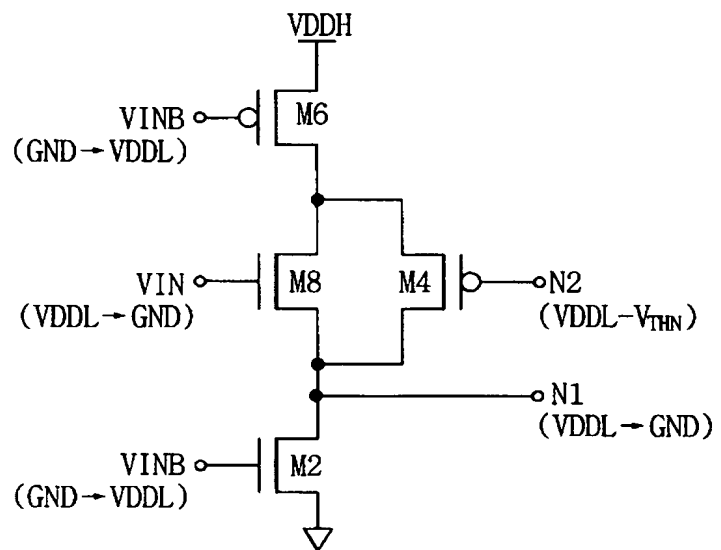


FIG. 5C

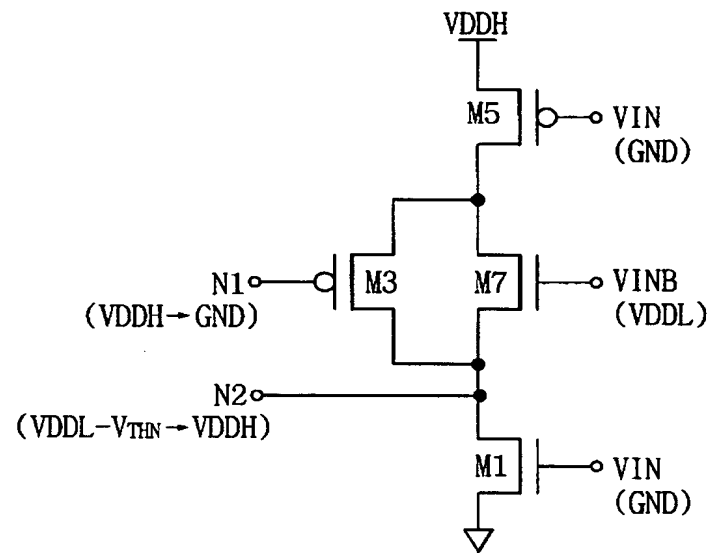


FIG. 5D

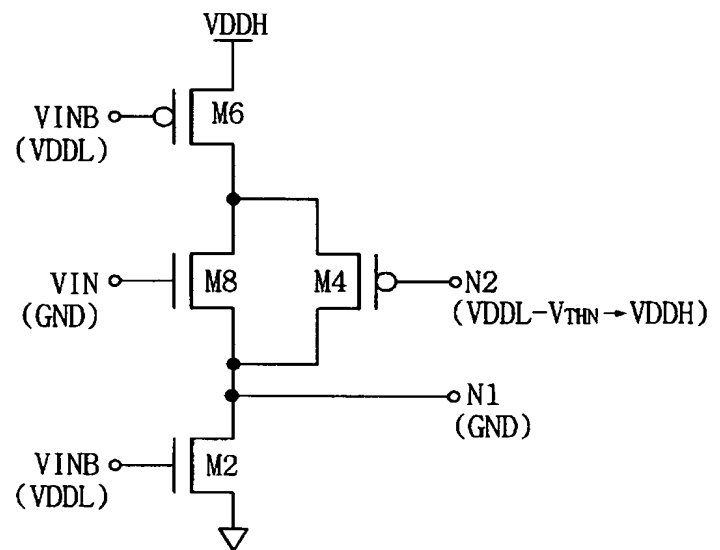


FIG. 6A

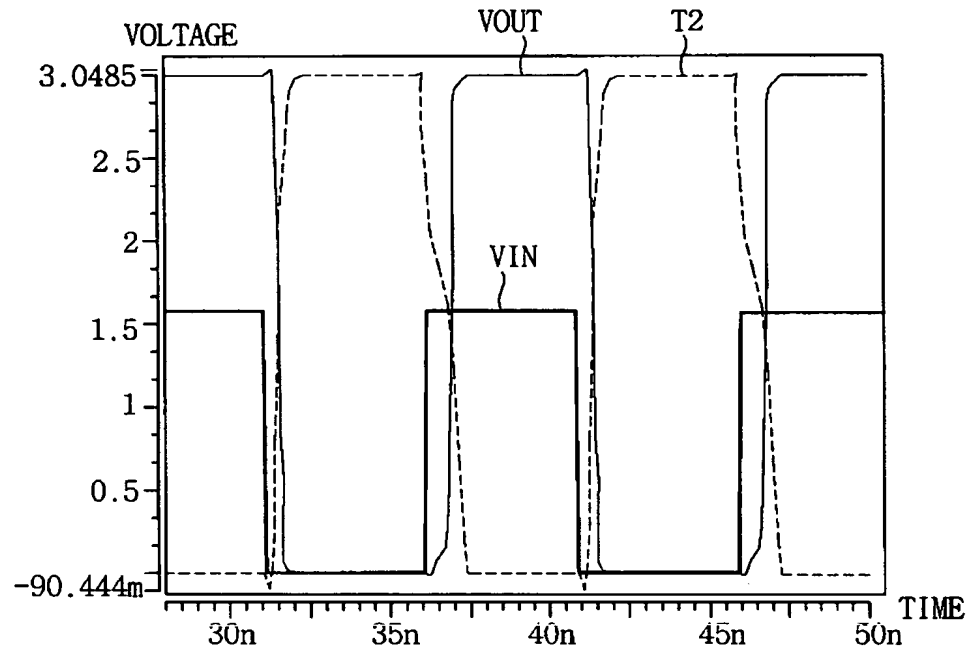


FIG. 6B

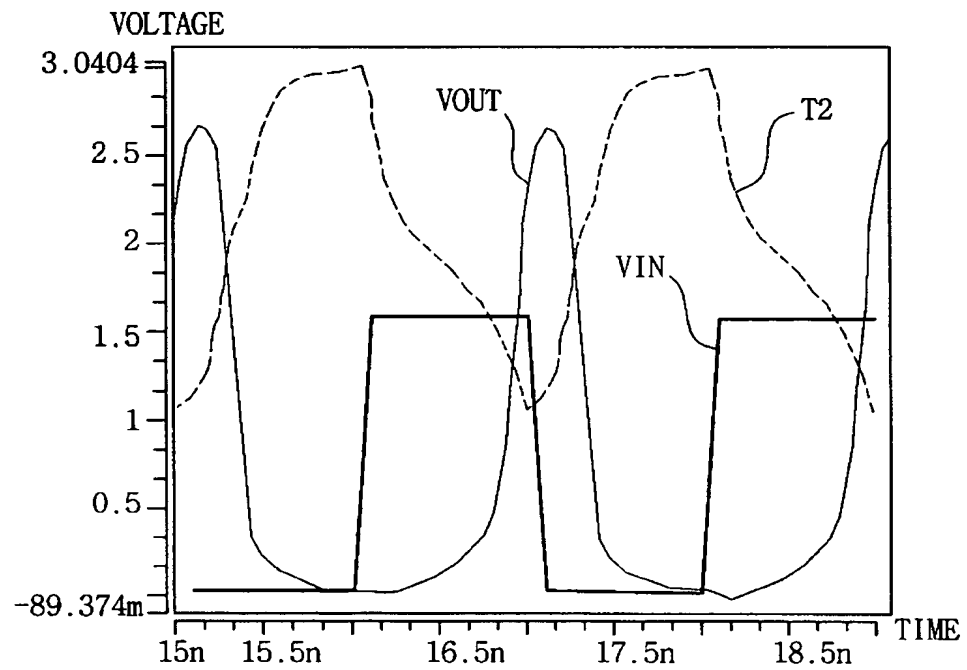


FIG. 6C

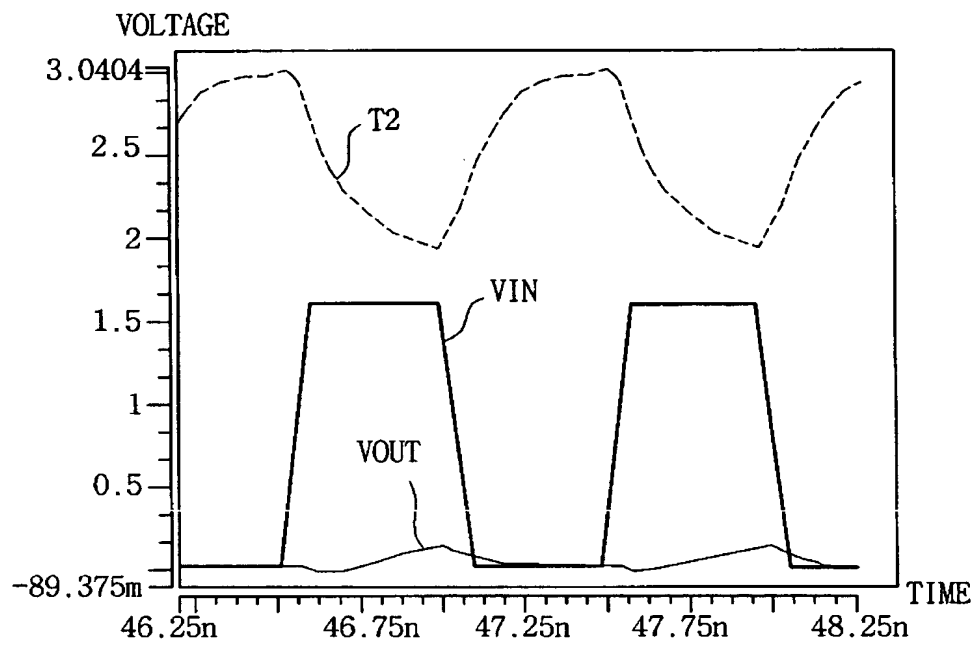


FIG. 7A

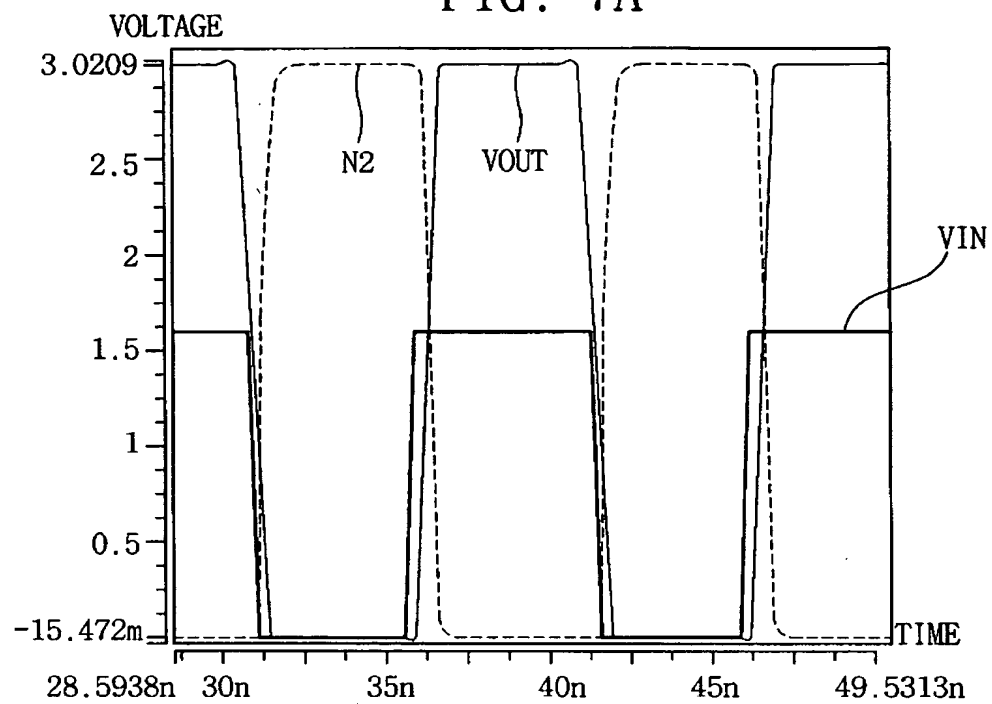


FIG. 7B

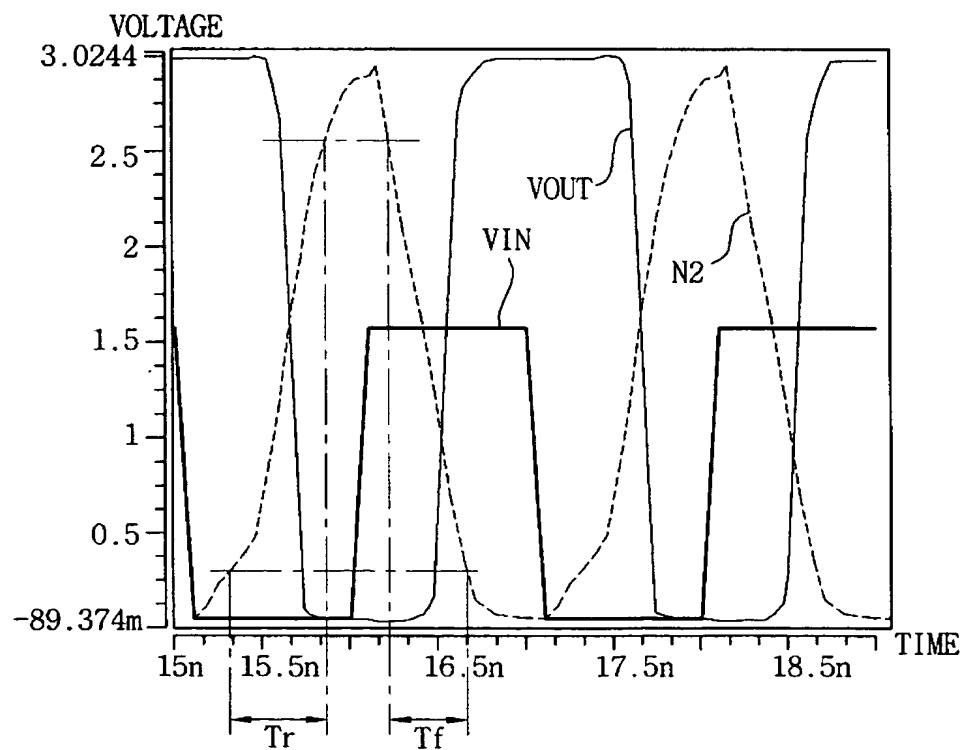




FIG. 7C

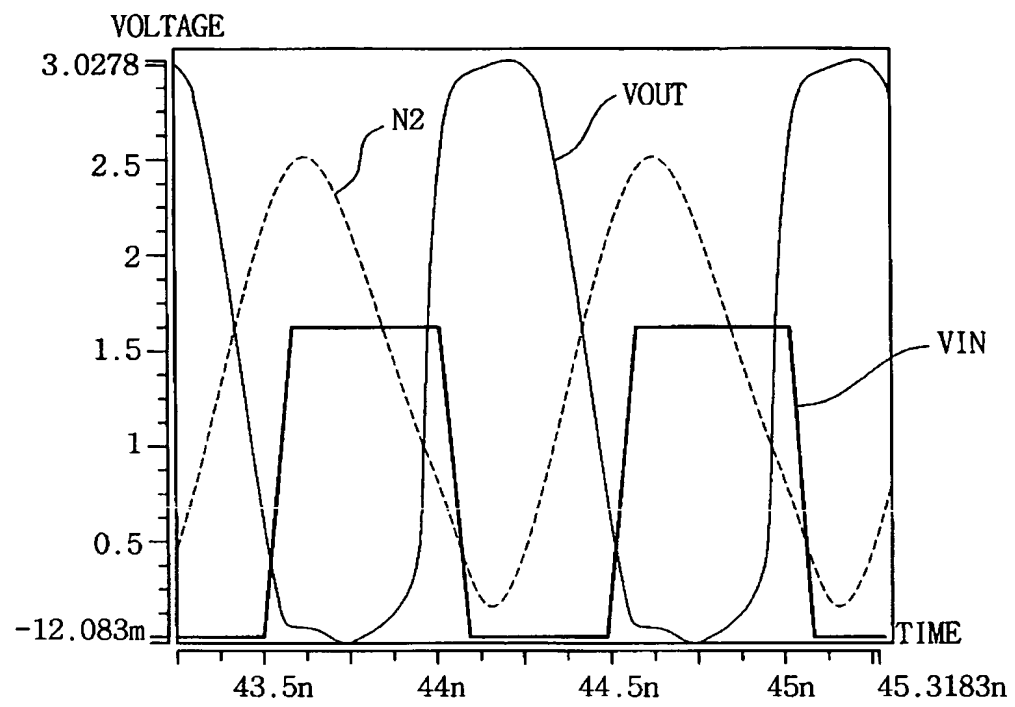
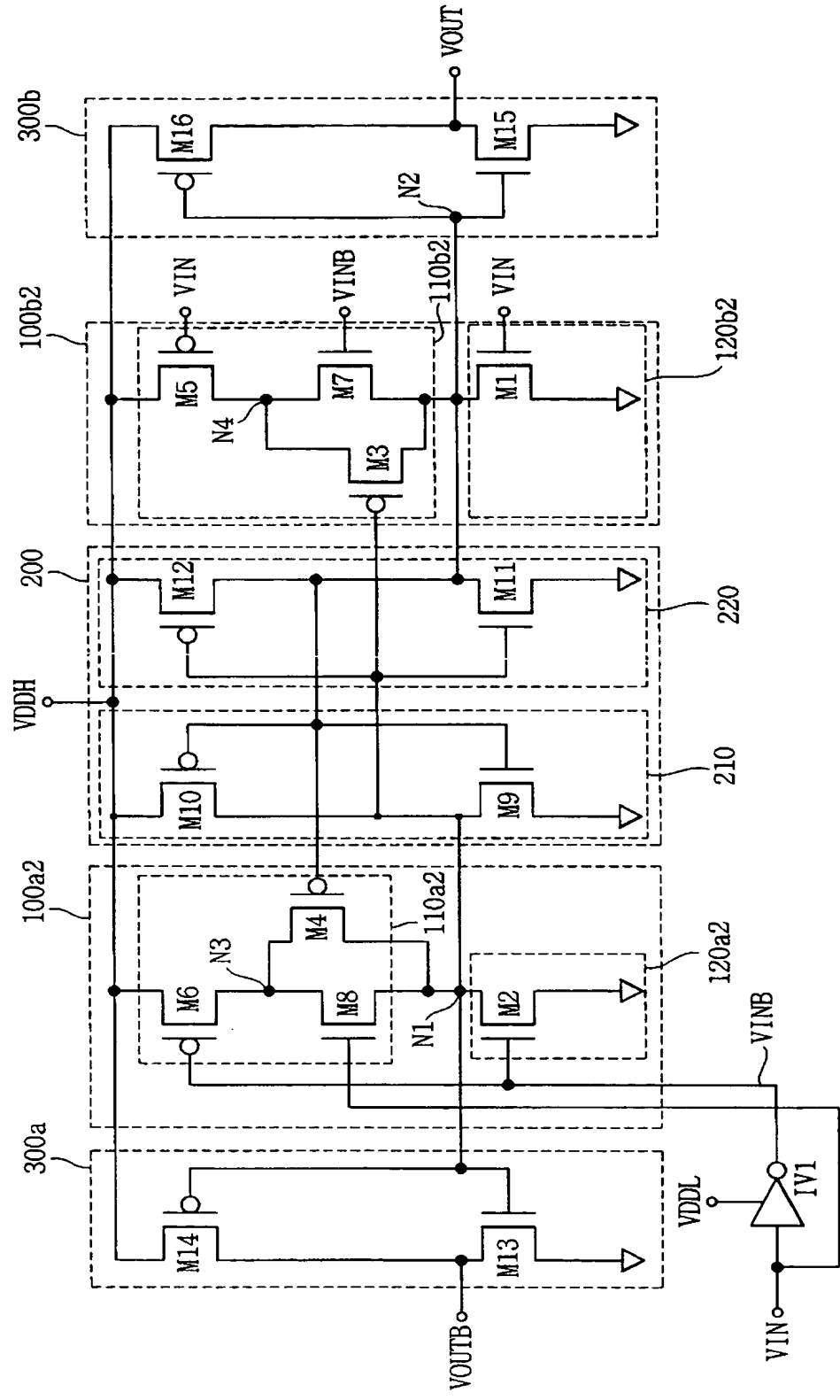


FIG. 8

		10MHz	100MHz	500MHz	1GHz
CONVENTIONAL STRUCTURE	SWING RANGE	100%	100%	89%	4%
	DUTY RATIO	49.5:50.5	46.5:53.5	18.3:81.7	-
	CURRENT (VDDH)	10uA	85uA	380uA	250uA
PRESENT INVENTION	SWING RANGE	100%	100%	100%	100%
	DUTY RATIO	49.9:50.1	49.0:51.0	48.5:52.0	51.2:48.8
	CURRENT (VDDH)	16uA	174uA	737uA	1089uA

FIG. 9



The circuit diagram illustrates a differential signal processing circuit with five stages, labeled 300a, 100a1, 200, 100b1, and 300b. The circuit is powered by a differential input signal VIN and a differential output signal VOUT. The input signal VIN is split into two paths: one path goes through a buffer (VINB) to the input of the first stage (300a), and the other path goes through a buffer (VINB) to the input of the fifth stage (300b). The output of the first stage (300a) is VOUTB, and the output of the fifth stage (300b) is VOUT. The circuit includes several transistors (M1-M16) and capacitors (N1-N4). The stages are interconnected in a differential manner, with the output of one stage being the input to the next stage. The circuit is designed to process differential signals and maintain a common-mode voltage (VDDH) for the input and output signals.

